4. (Amended) The non-volatile semiconductor according to claim 19, and further comprising an electric charge accumulating portion in an insulating layer having a trap level therein, said insulating layer being provided between said channel region and said control gate;

C4

wherein an erasing operation involves neutralization of electrons held by the trap level by injecting holes generated in the vicinity of said drain region.

6. (Amended) The non-volatile semiconductor according to claim 20, wherein said side wall comprises a first side wall and a second side wall formed on the first side wall, and wherein said drain region is formed in self-alignment with said first sidewall and said source region is formed in self-alignment with said second side wall.

C5

- Please add the following new claims 19-24:

19. (New) A non-volatile semiconductor memory comprising:

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a semiconductor substrate;

a source region provided in said semiconductor substrate;

a drain region provided in said semiconductor substrate, said source and drain regions being spaced away from each other;

a floating gate provided above a channel region between said source and drain regions; and

a control gate provided above said channel region;

wherein a writing operation is executed in such a way that hot electrons are generated in the vicinity of said drain region and injected into said floating gate, and an erasing operation is performed by releasing the electrons held by said floating gate into said channel region;

wherein an overlap of said drain region with said floating gate is larger than an overlap of said source region with said floating gate;

wherein said floating gate is provided between said channel region and said control gate through respective insulating layers; and

wherein a junction depth of said source region is larger than a junction depth of said drain region.

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20. (New) The non-volatile semiconductor memory according to claim 19, wherein at least said source region is provided by introducing an impurity in self-alignment with a side wall provided on a side surface of said control gate.

21. (New) A non-volatile semiconductor memory comprising:

a semiconductor substrate;

a source region provided in said semiconductor substrate; and

a drain region provided in said semiconductor substrate, said source and drain regions being spaced away from each other;

wherein a charge accumulation portion is an insulating layer having a trap level therein and said insulating layer is provided between said channel region and control gate and said control gate is provided above said channel region;

wherein a writing operation is executed in such a way that hot electrons are generated in the vicinity of said drain region and injected into said charge accumulation region and the erasing operation involves neutralization of the electrons held by the trap level by injecting holes generated at in the vicinity of said drain region;

wherein an overlap of said drain region with said electric charge accumulating portion is set larger than an overlap of said source region with said electric charge accumulating portion; and

wherein a junction depth of said source region is larger than a junction depth of said drain region.

22. (New) The non-volatile semiconductor memory according to claim 21, wherein at least said source region is provided by introducing an impurity in self-alignment with a side wall provided on a side surface of said control gate.

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23. (New) The non-volatile semiconductor memory according to claim 21, wherein an impurity dose quantity of said source region is larger than an impurity dose quantity of said drain region.

24. (New) The non-volatile semiconductor according to claim 22, wherein said side wall comprises a first side wall and a second side wall formed on the first side wall, and wherein said drain region is formed in self-alignment with said first sidewall and said source region is formed in self-alignment with said second side wall.

IN THE DRAWINGS:

Two new drawing sheets, comprising corrected Figs. 1 and 5, are submitted with this Amendment.